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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 09/430,366	Applicant(s) Ramsbey et al.
	Examiner Jack Chen	Group Art Unit 2813

☒ Responsive to communication(s) filed on *Jan 16, 2001*.

☒ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *1-12 and 14-20* is/are pending in the application.

Of the above, claim(s) *16-20* is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-12, 14, and 15* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐approved ☐disapproved.

☒ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☐ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

2. The amendment filed 1/16/2001 is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure. 35 U.S.C. 132 states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows: forming an oxide on exposed surfaces of the floating gate.

Applicant is required to cancel the new matter in the reply to this Office action.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 1 and 7 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. See above.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1-12, 14-15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Re claim 1, the phrase "forming an oxide on exposed surfaces of the floating gate" lack antecedent basis (not support by the specification), furthermore, it is also unclear "where" are the exposed surfaces of the floating gate; and "how" the exposed surfaces are formed.

Re claim 8, the term "the insulator" lacks antecedent basis.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

8. Claims 1, 2, 4-8, 10-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Chan et al., U.S./6,051,467.

Chan et al. discloses a method for forming a semiconductor device, which comprises providing a substrate 10; forming tunnel oxide 16 on the substrate; depositing a floating gate layer 18 on the tunnel oxide to first thickness; etching the floating gate layer to form floating gate 18 (fig. 2); forming an oxide 24 on exposed surfaces of the floating gate (fig. 3); depositing an insulator layer 30 on the substrate and the floating gate such that the insulator layer has a thickness that is greater than the first thickness (fig. 4); polishing the insulator layer to provide a planar surface that exposes a top surface of the floating gate and the insulator layer (fig. 5); and depositing a dielectric layer 36 (fig 7) on the planar surface over the exposed top surface of the floating gate and the insulator layer, figs. 1-11, cols. 1-8.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 3, 9, 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al. U.S./6,051,467 in view of Applicant's admitted prior art.

Chan et al. disclosed above, noting that figs. 1-11, cols. 1-8. However, the Chan et al. does not explicitly show using doped polysilicon or doped amorphous silicon for the floating gate.

It is well known in the art to use doped polysilicon or doped amorphous silicon for the floating gate, such will increase the conductivity of the floating gate (to lower the sheet resistance). For example, Applicant's admitted prior art teaches using doped polysilicon or doped amorphous silicon for the floating gate, see pages 1-2.

With respect to claims 3 and 9, the thickness of the layers are considered to involve routine optimization which has been held to the within the level of ordinary skill in art. Although the above references do not fall into the ranges of the inventor's disclosure, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to vary the thickness of the layers for optimization purposes. More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.

Furthermore, the implanting energy, dosage, thickness, width are considered to involve routine optimization which has been held to be within the level of ordinary skill in the art. As noted in In re Aller, the selection of reaction parameters such as energy, dosage, thickness, width and temperature, etc. would have been obvious:

> "Normally, it is to be expected that a change in energy, concentration, thickness, dosage, temperature, or combination of any of them would be an unpatentable modification. Under some circumstances, however, changes such as these may impart patentability to a

process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art...such ranges are termed "critical ranges and the applicant has the burden of proving such criticality.... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." *In re Aller 105 USPQ233, 255 (CCPA 1955). See also In re Waite 77 USPQ 586 (CCPA 1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmscher 66 USPQ 314 (CCPA 1945); In re Norman 66 USPQ 308 (CCPA 1945); In re Swenson 56 USPQ 372 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA 1935); In re Dreyfus 24 USPQ 52 (CCPA 1934).*

Therefore, one of ordinary skill in the requisite art at the time the invention was made would have used any thickness range suitable to the method in process of Chan et al. in order to optimize the process.

Furthermore, the subject matter as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify the standard process of Chan et al. with the teaching of Applicant's admitted prior art because of the desirability to improve device reliability and performance of the device (i.e. to lower the sheet resistance of the floating gate, etc.).

11. Claims 1-12, 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamauchi et al., U.S./5,962,889 or Wu, U.S./6,033,956 or Yamagishi et al., U.S./5,808,339

taken with Ogura et al., U.S./5,672,892 or Hong, U.S./5,478,767 in view of Applicant's admitted prior art.

Yamauchi et al. discloses a method for forming a semiconductor device, which comprises providing a substrate 1; forming tunnel oxide 2 on the substrate; depositing a floating gate layer on the tunnel oxide to first thickness; etching the floating gate layer to form floating gate 3; depositing an insulator layer on the substrate and the floating gate such that the insulator layer has a thickness that is greater than the first thickness; polishing the insulator layer to provide a planar surface that exposes a top surface of the floating gate and the insulator layer (fig. 14C); and depositing a dielectric layer 9 on the planar surface over the exposed top surface of the floating gate and the insulator layer, see figs. 1A-14E, cols. 1-14.

Wu discloses a method for forming a semiconductor device, which comprises providing a substrate 200; forming tunnel oxide 202 on the substrate; depositing a floating gate layer on the tunnel oxide to first thickness; etching the floating gate layer to form floating gate 204; depositing an insulator layer on the substrate and the floating gate such that the insulator layer has a thickness that is greater than the first thickness; polishing the insulator layer to provide a planar surface that exposes a top surface of the floating gate and the insulator layer (fig. 2C); and depositing a dielectric layer 214 on the planar surface over the exposed top surface of the floating gate and the insulator layer, see figs. 1-4G, cols. 1-6.

Yamagishi et al. discloses a method for forming a semiconductor device, which comprises providing a substrate 11; forming tunnel oxide 51 on the substrate; depositing a floating gate layer

on the tunnel oxide to first thickness; etching the floating gate layer to form floating gate 53; depositing an insulator layer 54 on the substrate and the floating gate such that the insulator layer has a thickness that is greater than the first thickness; polishing the insulator layer to provide a planar surface that exposes a top surface of the floating gate and the insulator layer (figs. 10A-10B); and depositing a dielectric layer 55 on the planar surface over the exposed top surface of the floating gate and the insulator layer, see figs. 1-12B, cols. 1-16.

However, the above references do not explicitly show using doped polysilicon or doped amorphous silicon for the floating gate, and forming an oxide on exposed surfaces of the floating gate.

It is well known in the art to use doped polysilicon or doped amorphous silicon for the floating gate, such will increase the conductivity of the floating gate. For example, Applicant's admitted prior art teaches using doped polysilicon or doped amorphous silicon for the floating gate, see pages 1-2. It is also well known in the art to thermally oxidizing the floating gate to seal the vertical surfaces of the floating gate such will provide isolation (forming an oxide on exposed surfaces of the floating gate to eliminate short circuit, etc.) from the adjacent gates or device elements, and keep charges within the floating gate. For example, Ogura et al. teaches thermally oxidizing the floating gate to seal the vertical surfaces of the floating gate, see figs. 1-5, cols. 1-16; Hong also teaches thermally oxidizing the floating gate to seal the vertical surfaces of the floating gate, see figs. 1-4K, cols. 1-10.

With respect to claims 3 and 9, the thickness of the layers are considered to involve routine optimization which has been held to the within the level of ordinary skill in art. Although the above references do not fall into the ranges of the inventor's disclosure, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to vary the thickness of the layers for optimization purposes. More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.

Furthermore, the implanting energy, dosage, thickness, width are considered to involve routine optimization which has been held to be within the level of ordinary skill in the art. As noted in In re Aller, the selection of reaction parameters such as energy, dosage, thickness, width and temperature, etc. would have been obvious:

> "Normally, it is to be expected that a change in energy, concentration, thickness, dosage, temperature, or combination of any of them would be an unpatentable modification. Under some circumstances, however, changes such as these may impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art...such ranges are termed "critical ranges and the applicant has the burden of proving such criticality.... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation."

In re Aller 105 USPQ233, 255 (CCPA 1955). See also In re Waite 77 USPQ 586 (CCPA 1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmscher 66 USPQ 314 (CCPA 1945); In re Norman 66 USPQ 308 (CCPA 1945); In re Swenson 56 USPQ 372 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA 1935); In re Dreyfus 24 USPQ 52 (CCPA 1934).

Therefore, one of ordinary skill in the requisite art at the time the invention was made would have used any energy, concentration, thickness, width range suitable to the method in process of Yamauchi et al., U.S./5,962,889 or Wu, U.S./6,033,956 or Yamagishi et al., U.S./5,808,339 in order to optimize the process.

Furthermore, the subject matter as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify the standard process of Yamauchi et al. or Wu or Yamagishi et al. with the teaching of (Ogura et al. or Hong) and Applicant's admitted prior art because of the desirability to improve device reliability and performance of the device.

Response to Arguments

12. Applicant's arguments filed 1/16/2001 have been fully considered but they are not persuasive.

Applicant argues that the prior art (Chan et al., U.S./6,051,467) does not show "depositing a dielectric layer ***on*** the plannar surface ***over*** the exposed top surface of the floating gate and the insulator" the Examiner disagrees because fig. 7 clearly shows this feature;

Yamagishi et al. also show this feature in fig. 10B; Wu also shows this feature in fig. 2D; and Yamauchi et al. also shows this feature in fig. 14D.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., use the oxide to achieve high registration for ...and to prevent charge leakage) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

13. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jack Chen whose telephone number is (703) 308-5838. The examiner can normally be reached on Monday-Friday from 8:30 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Bowers, can be reached on (703) 308-2417.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Jack Chen

April 5, 2001

Charles Bowers
Supervisory Patent Examiner
Technology Center 2800